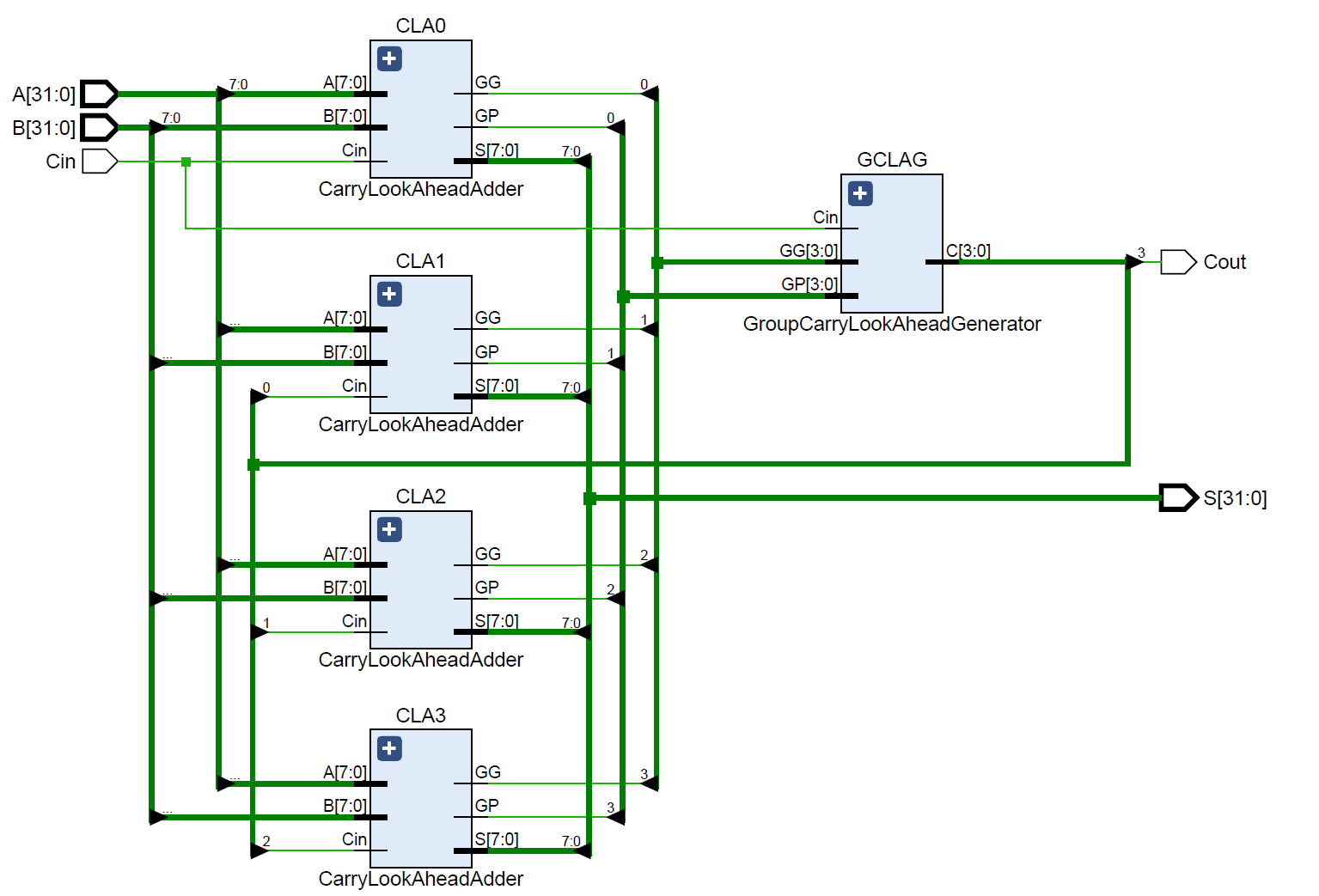
# CLA Adder

## Block Diagram



**For 8-bit CLA adder,**

Carry Generate:

Carry Propagate:

Sum:

**For 32-bit CLA adder, we used four 8-bit CLA adders with Group CLA Generator.**

Group Carry Generate:

Group Carry Propagate:

///see reference pdf in the reference folder.

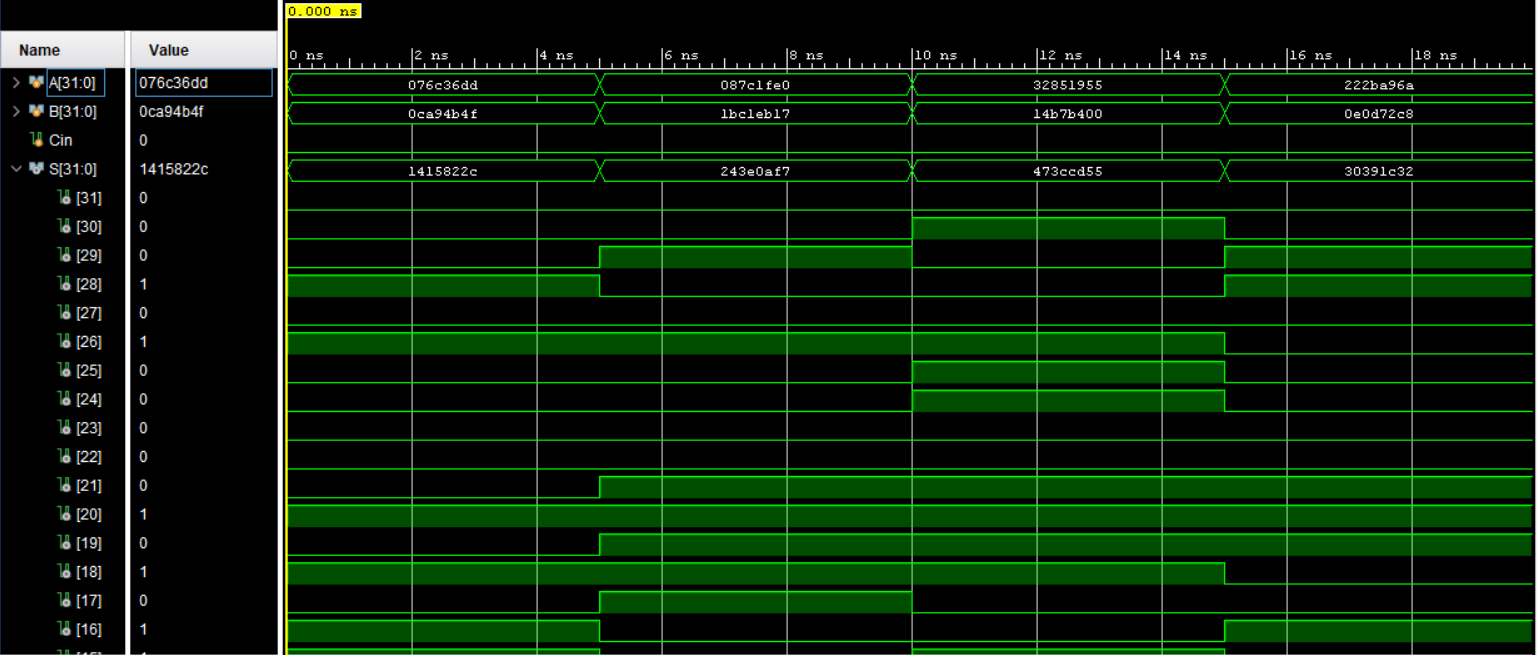
## Propagation Time Estimation

## Time Taken to add 4 pairs of numbers

## Verilog Code

---*code snap---*

## Simulation Result



Add 4 numbers with 5ns time gap. Since this is a simulation, we cannot see the propagation delay of CLA adder.